27 Lecture - CS302

Important Mcqs

1. **What is a down counter?**
   a) A digital circuit that counts up from a specified initial value to a maximum value
   b) A digital circuit that counts down from a specified initial value to zero
   c) A digital circuit that counts up or down depending on the input signal
   d) A digital circuit that counts at a constant rate
   Answer: b) A digital circuit that counts down from a specified initial value to zero

   Which type of counter is commonly used in synchronous down counters?
   a) Flip-flops
   b) Schmitt triggers
   c) Shift registers
   d) Multiplexers
   Answer: a) Flip-flops

   What is the maximum count that a 4-bit down counter can achieve?
   a) 7
   b) 8
   c) 15
   d) 16
   Answer: b) 8

   What is the purpose of a presettable down counter?
   a) To count down from a specified initial value
   b) To count up to a specified final value
   c) To count up or down depending on the input signal
   d) To count at a constant rate
   Answer: a) To count down from a specified initial value

   Which type of down counter is also known as a binary ripple counter?
   a) Synchronous down counter
   b) Asynchronous down counter
   c) Presettable down counter
   d) Decade counter
   Answer: b) Asynchronous down counter

   Which input signal is used to enable a down counter?
   a) Clock
   b) Clear
   c) Load
   d) Count
   Answer: a) Clock

   Which type of down counter is commonly used in frequency dividers?

a) Synchronous down counter
b) Asynchronous down counter
c) Presettable down counter
d) Decade counter
Answer: a) Synchronous down counter

What is the output of a down counter when the count reaches zero?
a) High
b) Low
c) Depends on the circuit design
d) No output
Answer: b) Low

Which statement is true for a down counter with an active-high clock input?
a) The count decreases on the rising edge of the clock
b) The count decreases on the falling edge of the clock
c) The count increases on the rising edge of the clock
d) The count increases on the falling edge of the clock
Answer: b) The count decreases on the falling edge of the clock

Which statement is true for a down counter with an active-low clear input?
a) The counter is cleared on the rising edge of the clear input
b) The counter is cleared on the falling edge of the clear input
c) The counter is not affected by the clear input
d) The counter is cleared when the clear input is high
Answer: d) The counter is cleared when the clear input is high