

# 28 Lecture - CS302

## Important Mcqs

1. In a synchronous decade counter, how many flip-flops are used?

- a) 4
- b) 6
- c) 8
- d) 10

Answer: d) 10

What is the maximum count of a synchronous decade counter?

- a) 5
- b) 9
- c) 10
- d) 16

Answer: c) 10

What is the clock signal frequency required for a synchronous decade counter to count at 1 Hz?

- a) 1 kHz
- b) 10 kHz
- c) 100 kHz
- d) 1 MHz

Answer: b) 10 kHz

How many clock cycles are required for a synchronous decade counter to count from 0 to 5?

- a) 3
- b) 5
- c) 10
- d) 16

Answer: b) 5

What is the purpose of the carry output in a synchronous decade counter?

- a) to indicate when the counter has reached its maximum count
- b) to provide a clock signal for the next stage of the counter
- c) to reset the counter to its initial value
- d) to enable/disable the counter

Answer: b) to provide a clock signal for the next stage of the counter

What is the relationship between the clock signal and the flip-flop outputs in a synchronous decade counter?

- a) they are always in phase with each other
- b) they are always out of phase with each other
- c) they are in phase during the count up and out of phase during the count down
- d) they are out of phase during the count up and in phase during the count down

Answer: a) they are always in phase with each other

What is the timing relationship between the flip-flop outputs in a synchronous decade

**counter?**

- a) they change state simultaneously on the rising edge of the clock signal
- b) they change state simultaneously on the falling edge of the clock signal
- c) they change state sequentially on the rising edge of the clock signal
- d) they change state sequentially on the falling edge of the clock signal

**Answer: c) they change state sequentially on the rising edge of the clock signal**

**What is the timing relationship between the carry output and the flip-flop outputs in a synchronous decade counter?**

- a) the carry output is always one clock cycle ahead of the flip-flop outputs
- b) the carry output is always one clock cycle behind the flip-flop outputs
- c) the carry output and the flip-flop outputs change state simultaneously
- d) the carry output and the flip-flop outputs change state alternately

**Answer: b) the carry output is always one clock cycle behind the flip-flop outputs**

**What is the maximum frequency of a synchronous decade counter with a 50 ns propagation delay per flip-flop?**

- a) 20 kHz
- b) 50 kHz
- c) 100 kHz
- d) 200 kHz

**Answer: c) 100 kHz**

**How many clock cycles are required for a synchronous decade counter to count from 9 to 0?**

- a) 1
- b) 9
- c) 10
- d) 20

**Answer: c) 10**