

# 28 Lecture - CS302

## Important Subjective

1. **What is a timing diagram of a synchronous decade counter, and what does it represent?**

Answer: A timing diagram of a synchronous decade counter is a graphical representation of the timing relationship between the clock signal, the flip-flop outputs, and the counter output. It shows how the counter advances by one on each clock pulse and how the flip-flop outputs change state to reflect the new counter value. It also shows the ripple effect of the carry output from one flip-flop to the next and how this results in a delay in the counter output.

**How does the timing diagram of a synchronous decade counter differ from that of an asynchronous counter?**

Answer: The timing diagram of a synchronous decade counter shows that all flip-flops receive the same clock signal and change state simultaneously. In contrast, the timing diagram of an asynchronous counter shows that each flip-flop receives a delayed clock signal from the previous flip-flop, and therefore the flip-flops change state sequentially.

**How can you use a timing diagram to verify the performance of a synchronous decade counter?**

Answer: A timing diagram can be used to verify the performance of a synchronous decade counter by comparing the counter output with the expected sequence of values. If the counter output matches the expected sequence, then the counter is functioning correctly.

**What is the purpose of the carry output in a synchronous decade counter, and how is it represented in the timing diagram?**

Answer: The carry output in a synchronous decade counter is used to provide a clock signal for the next stage of the counter. It is represented in the timing diagram as a delayed pulse that occurs after the flip-flop outputs have changed state.

**What is the maximum count of a synchronous decade counter, and how many flip-flops are used to achieve this count?**

Answer: The maximum count of a synchronous decade counter is 10, and 10 flip-flops are used to achieve this count.

**How many clock cycles are required for a synchronous decade counter to count from 0 to 5?**

Answer: 5 clock cycles are required for a synchronous decade counter to count from 0 to 5.

**What is the timing relationship between the clock signal and the flip-flop outputs in a synchronous decade counter?**

Answer: The clock signal and the flip-flop outputs are always in phase with each other in a synchronous decade counter.

**What is the timing relationship between the flip-flop outputs in a synchronous decade counter?**

Answer: The flip-flop outputs change state sequentially on the rising edge of the clock signal in

a synchronous decade counter.

**What is the propagation delay of a flip-flop, and how does it affect the maximum frequency of a synchronous decade counter?**

Answer: The propagation delay of a flip-flop is the time it takes for the output to change state after a clock edge. It affects the maximum frequency of a synchronous decade counter because the delay adds up as the clock signal propagates through each flip-flop, limiting the maximum clock frequency that can be used.

**How can you calculate the maximum clock frequency of a synchronous decade counter given the propagation delay of each flip-flop?**

Answer: The maximum clock frequency of a synchronous decade counter can be calculated by dividing the minimum propagation delay of the flip-flops by the number of flip-flops used. For example, if each flip-flop has a minimum propagation delay of 20 ns and 10 flip-flops are used, the maximum clock frequency would be  $1/(20\text{ns} \times 10) = 500 \text{ kHz}$ .